



VARISCITE LTD.

VAR-SOM-AM33 V1.0 Datasheet

Texas Instruments Sitara AM335x-based System-on-Module

Rev: 1.01



VARISCITE LTD.

VAR-SOM-AM33 Datasheet

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Table of Contents

Document Revision History	iii
Table of Contents	iv
List of Tables	7
1 Overview	8
1.1 General Information	8
1.2 Features Summary	9
1.3 Block Diagram	10
2 Main Hardware Components	11
2.1 Texas Instruments Sitara AM335x	11
2.1.1 Overview	11
2.1.2 Sitara AM335x Block Diagram	12
2.1.3 Detailed Description	12
2.1.3.1 MPU Subsystem	12
2.1.3.2 External Memory Interfaces	13
2.1.3.2.1 GPMC	13
2.1.3.2.2 EMIF Module:	14
2.1.3.3 LCD Controller	14
2.1.3.4 2D and 3D Graphics Accelerator (SGX)	15
2.1.3.5 Multichannel Audio Serial Port (McASP)	16
2.1.3.6 Ethernet Subsystem	17
2.1.3.7 Universal Serial BUS	18
2.2 Memory	19
2.2.1 RAM	19
2.2.2 Non-volatile Storage Memory	19
2.3 On-board Ethernet PHY	19
2.4 TLV320AIC3106 Audio	19
2.5 TPS65910 PMIC	19
3 External Connectors	20
3.1 SoM Connector Pin-out	20
3.2 SO-DIMM 200 Pin Mux	27
4 Interface Details	30
4.1 Overview	30
4.2 Display Interfaces	30
4.3 Ethernet	31
4.3.1 10/100 Base-T Interface	31
4.3.2 Ethernet PHY Features	31
4.3.3 Gigabit Ethernet	31
4.3.4 RGMII Signals	32

4.4	USB HOST 2.0	33
4.4.1	USB Host Signals	33
4.5	USB 2.0 On-the-Go	33
4.5.1	OTG Signals	33
4.6	MMC/SD/SDIO	33
4.6.1	MMC/SD/SDIO Features	33
4.6.2	SDMMC0 Signals	34
4.6.3	SDMMC1 Signals	34
4.7	Audio	34
4.7.1	Audio CODEC	34
4.7.3	McASP	35
4.8	UART Interfaces	35
4.8.1	UART Features	35
4.8.2	UART0 Signals	36
4.8.3	UART1 Signals	36
4.8.4	UART3 Signals	36
4.9	SPI	36
4.9.1	SPI Features	37
4.9.2	McSPI1 Signals	37
4.10	I ² C	38
4.10.1	I ² C Features	38
4.10.2	I2C0 Signals	39
4.10.3	I2C0 Address Mapping	39
4.10.4	I2C1 Signals	39
4.11	PWM0	39
4.11.1	PWM0 Signal	39
4.12	Local Bus	39
4.12.1	GPMC Features	39
4.13	Touch Screen	40
4.13.1	ADC Features	40
4.13.2	Touch-screen Controller Signals	40
4.14	General Purpose IOs	41
4.14.1	Default GPIO Signals	41
4.15	General System Control	41
4.15.1	Boot Options	41
4.15.2	SYS_RESETn	41
4.15.3	VCC3V3	41
4.15.4	General System Control Signals	41
4.16	Power	43
4.16.1	Power Supply	43
4.16.2	Ground	43
5	Absolute Maximum Characteristics	44
6	Operational Characteristics	44

6.1	Power supplies	44
6.2	Power Consumption	44
7	DC Electrical Characteristics	44
8	Environmental Specifications	45
9	Mechanical Drawings	46
10	Legal Notice	47
11	Warranty Terms	48
12	Contact Information.....	49

List of Tables

Table 3-1 SO-DIMM200 Pin Out	26
Table 3-2 SO-DIMM 200 Pin MuX.....	29
Table 4-1 Display Signals.....	31
Table 4-2 Ethernet Signals	31
Table 4-3 Ethernet Signals	32
Table 4-4 USB Host1 Signals	33
Table 4-5 USB OTG Signals	33
Table 4-6 SDMMC0 Signals.....	34
Table 4-7 SDMMC1 Signals.....	34
Table 4-8 Audio Signals	35
Table 4-9 UART0 Signals	36
Table 4-10 UART1 Signals	36
Table 4-11 UART3 Signals.....	36
Table 4-12 SPI Signals	37
Table 4-13 I2C0 Signals	39
Table 4-14 I2C0 Address Mapping.....	39
Table 4-21 I2C1 Signals	39
Table 4-16 PWM0 Signal.....	39
Table 4-17 Touch Panel Signals.....	41
Table 4-26 General System Signals.....	42
Table 4-27 Power Supply Pins	43
Table 4-28 Ground Pins	43
Table 5-1 Absolute Maximum Characteristics	44
Table 6-1 Power Supplies Operational Characteristics	44
Table 7-1 DC Electrical Characteristics	44

1 Overview

1.1 General Information

The VAR-SOM-AM33 is a high performance, highly integrated, compact, low power consumption and low cost System-on-Module. It provides an ideal building block that easily integrates with a wide range of target markets, such as medical devices, industrial control and other applications requiring reach connectivity features as well as high-processing power.

Supporting products:

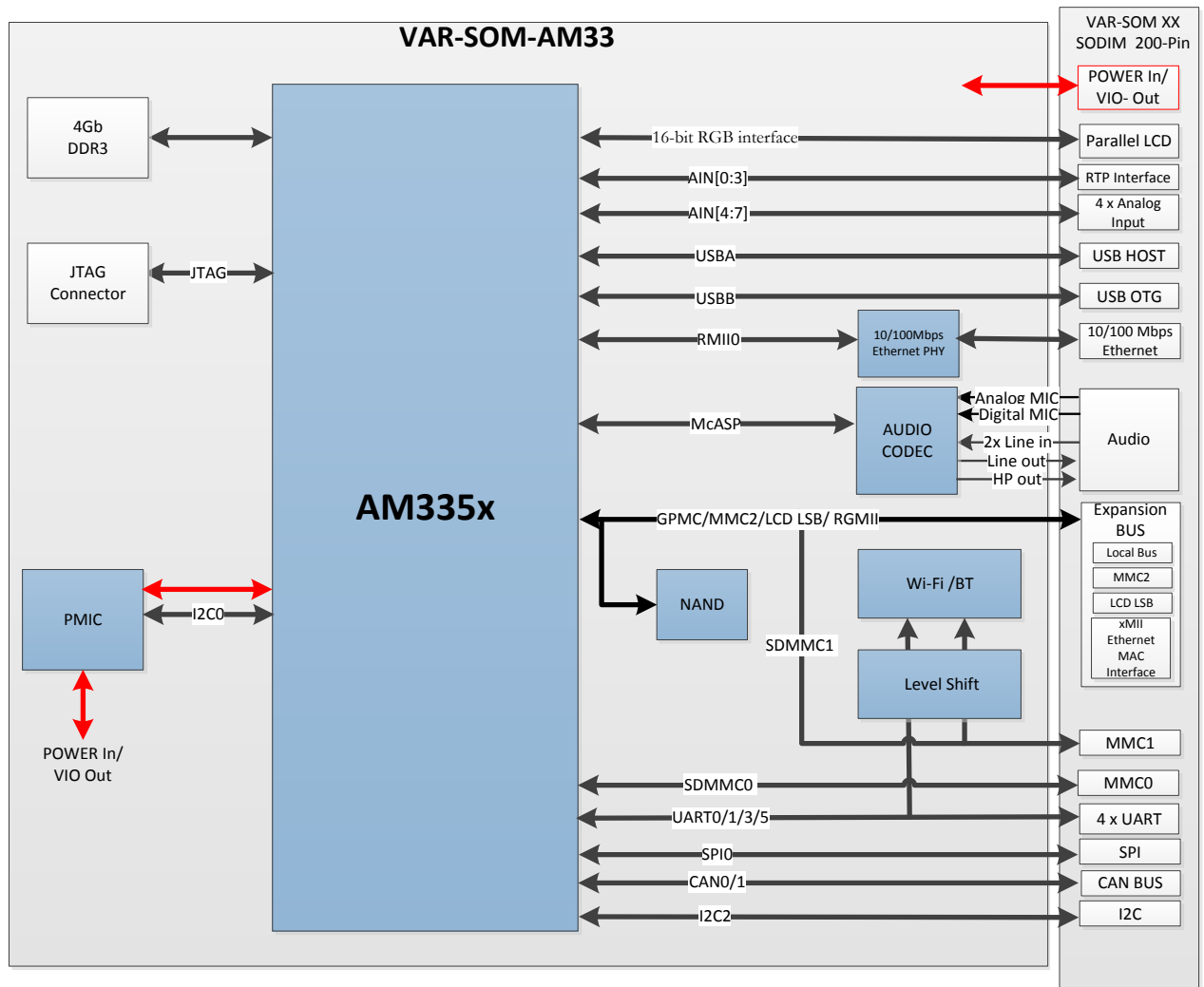
- VAR-AM33CustomBoard – evaluation board
 - ✓ Carrier-board, compatible with VAR-SOM-AM33
 - ✓ Schematics
- OS support
 - ✓ Linux BSP
 - ✓ Windows Embedded Compact 7
 - ✓ Android

Contact Variscite support services for further information:
[mail to: support@variscite.com](mailto:support@variscite.com).

1.2 Features Summary

- TI's Sitara AM335x:
 - 600-MHz, or 720-MHz ARM® Cortex™-A8
 - NEON™ SIMD coprocessor
 - SGX530 graphics engine
- Up to 4 Gb DDR3 RAM
- Up to 4 Gb NAND Flash for storage memory / boot
- LCD interface (up to 24-bit parallel RGB)
- Touch panel interface
- On-board 10/100 Mbps Ethernet PHY
- 10/100/1000 M bps Ethernet MAC (xMII Interface)
- WLAN (802.11 b/g/n)
- USB:
 - 1 x USB 2.0 host
 - 1 x USB 2.0 OTG
- 2 X CAN bus
- Serial interfaces (SPI, I2C, UART)
- Audio:
 - 2 x stereo line-in
 - 2 x stereo line-out
 - 1 x headphone-out
 - 1 x microphone-in
 - Digital microphone interface
 - Multichannel Audio Serial Port (McASP)
- ADC
- Single 3.3 V power supply
- 6.73 mm x 3.86 mm x 3 mm SO-DIMM footprint

1.3 Block Diagram



2 Main Hardware Components

This section summarizes the main hardware building blocks of the VAR-SOM-AM33

2.1 Texas Instruments Sitara AM335x

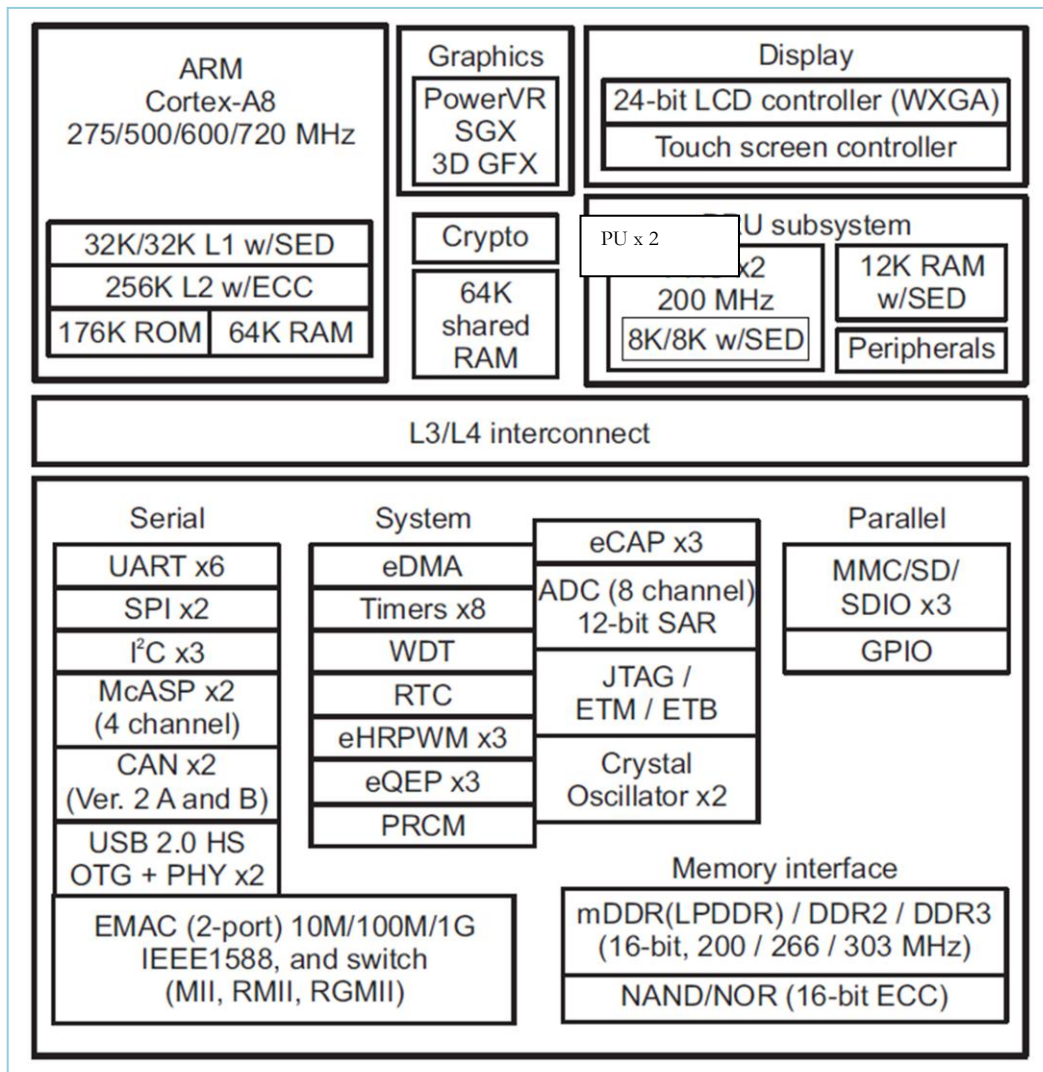
2.1.1 Overview

The AM335x microprocessors based on the ARM Cortex-A8 are enhanced with image, graphics processing, peripherals and industrial interface options.

The AM335x microprocessor contains the following subsystems, controller and interfaces:

- Microprocessor unit (MPU) subsystem based on the ARM Cortex-A8 microprocessor(275-MHz, 500-MHz, 600-MHz, or 720-MHz options)
- POWERVR SGX™530 graphics accelerator subsystem for 3D graphics acceleration to support display and gaming effects
- Programmable Real-time Unit SubSystem (PRUSS) enables the user to create a variety of digital resources beyond the native peripherals of the device.
- Memory Subsystem (GPMC)
- LCD controller
- Touch screen controller
- USB 2.0 OTG ports
- 10/100/1000 Ethernet, featuring wire speed switching
- MultiMediaCard (MMC) controller
- Multichannel Audio Serial Port (McASP)
- Controller Area Network (CAN)
- Multichannel Serial Port (McSPI)
- Universal Asynchronous Rx/Tx (UART)

2.1.2 Sitara AM335x Block Diagram



2.1.3 Detailed Description

2.1.3.1 MPU Subsystem

The MPU subsystem key features are:

- ARM Microprocessor
 - CortexA8
 - ARM Architecture version 7 ISA.
 - 2-issue, in-order execution pipeline.
 - L1 and L2 Instruction and Data Cache of 32 KB , 4-way, 16 word line with 128 bit interface.
 - Integrated L2 cache of 256 KB, 8-way, 16 word line, and 128 bit interface to L1 along with ECC/Parity supported.
 - Includes the Neon Media coprocessor (NEON™) which implements the Advanced SIMD media processing architecture.
 - Includes the VFP coprocessor which implements the VFPv3 architecture and is fully compliant with IEEE 754 standard.

- The external interface uses the AXI protocol configured to 128-bit data width.
- Includes the Embedded Trace Macrocell (ETM) support for non-invasive debugging.
- Implements the ARMv7 debug with watch-point and breakpoint registers and 32-bit Advanced Peripheral Bus (APB) slave interface to CoreSight debug systems.
- AXI2OCP Bridge
 - Support OCP 2.2.
 - Single Request Multiple Data Protocol on two ports.
 - Multiple targets, including three OCP ports (128-bit, 64-bit and 32-bit).
- Interrupt Controller
 - Support up to 128 interrupt requests
- Emulation/Debug
 - Compatible with CoreSight Architecture.
- Clock Generation
 - Through PRCM
- DFT
 - Integrated PBIST controller to test L2 tag and data ram, L1I and L1D data ram and OCM RAM

2.1.3.2 External Memory Interfaces

AM335x memory subsystem main interfaces are

- GPMC
- EMIF

2.1.3.2.1 GPMC

The general features of the GPMC module include:

- Data path to external memory device can be 16- or 8-bit wide
- 32-bit OCPIP 2.0 compliant core, single slave interface. Support non-wrapping and wrapping burst up to 16x32bits.
- Up to 100 MHz external memory clock performance (single device)
- Support for the following memory types:
 - External asynchronous or synchronous 8-bit width memory or device (non-burst device)
 - External asynchronous or synchronous 16-bit width memory or device
 - External 16-bit non-multiplexed NOR Flash device
 - External 16-bit address and data multiplexed NOR Flash device
 - External 8-bit and 16-bit NAND flash device
 - External 16-bit pSRAM device
- Up to 16-bit ECC support for NAND flash using BCH code (t=4, 8 or 16) or Hamming code for 8-bit or 16-bit NAND-flash, organized with page size of 512 bytes, 1K bytes, or more.
- Support 512M Bytes maximum addressing capability which can be divided into seven independent chip-select with programmable bank size and base address on 16M Bytes, 32M Bytes, 64M Bytes, or 128M Bytes boundary.
- Fully pipelined operation for optimal memory bandwidth usage

- Support external device clock frequency of 1, 2, 3 and 4 divider from L3 clock.
- Support programmable auto-clock gating when there is no access.
- Support Midlreq/SidleAck protocol
- Support the following interface protocols when communicating with external memory or external devices.
 - Asynchronous read/write access
 - Asynchronous read page access (4-8-16 Word16)
 - Synchronous read/write access
 - Synchronous read burst access without wrap capability (4-8-16 Word16)
 - Synchronous read burst access with wrap capability (4-8-16 Word16)
- Address and Data multiplexed access
- Each chip-select as independent and programmable control signal timing parameters for Setup and Hold time. Parameters are set according to the memory device timing parameters, with one L3 clock cycle timing granularity.
- Flexible internal access time control (wait state) and flexible handshake mode using external WAIT pins monitoring (up to two WAIT pins).
- Support bus keeping
- Support bus turn around

2.1.3.2.2 EMIF Module:

The EMIF module provides connectivity between the device and the DDR3 memories, while managing data bus read/write access between external memories, the microprocessor unit (MPU) and the direct memory access (DMA) controller

2.1.3.3 LCD Controller

The LCD controller Main features are

- Supports up to 24-bit data output; 8 bits-per-pixel (RGB).
- Supports up to WXGA resolution.
- Integrated DMA engine to pull data from the external frame buffer without burdening the processor via Interrupts or a firmware timer.
- 512 word deep internal FIFO with programmable threshold values.
- Character Based Panels
 - Supports 2 Character Panels (CS0 and CS1) with independent and programmable bus timing parameters when in asynchronous Hitachi, Motorola and Intel modes
 - Supports 1 Character Panel (CS0) with programmable bus timing parameters when in synchronous Motorola and Intel modes
 - Can be used as a generic 16 bit address/data interleaved MPU bus master with no external stall
- Passive Matrix LCD Panels
 - Panel types including STN, DSTN, and C-DSTN
 - AC Bias Control
- Active Matrix LCD Panels
 - Panel types including TN TFT
- OLED Panels

- Passive Matrix (PM OLED) with frame buffer and controller IC inside the Panel
- Active Matrix (AM OLED)

2.1.3.4 2D and 3D Graphics Accelerator (SGX)

The 2D/3D graphics accelerator (SGX) subsystem accelerates 2-dimensional (2D) and 3-dimensional (3D) graphics applications. The SGX subsystem is based on the POWERVR® SGX core from Imagination Technologies. SGX is a new generation of programmable POWERVR graphic cores. The POWERVR SGX530 v1.2.5 architecture is scalable and can target all market segments from mainstream mobile devices to high-end desktop graphics. Targeted applications include feature phone, PDA and hand-held games.

POWERVR SGX main features:

- 2D graphics, 3D graphics, vector graphics and programming support for GP-GPU functions
- Tile-based architecture
- Universal scalable shader engine (USSE™) – multithreaded engine incorporating pixel and vertex shader functionality
- Advanced shader feature set – in excess of Microsoft VS3.0, PS3.0, and OpenGL2.0
- Industry-standard API support – Direct3D Mobile, OpenGL ES 1.1 and 2.0, OpenVG v1.0.1
- Fine-grained task switching, load balancing, and power management
- Advanced geometry direct memory access (DMA) driven operation for minimum CPU interaction
- Programmable high-quality image anti-aliasing
- POWERVR SGX core MMU for address translation from the core virtual address to the external physical address (up to 4GB address range)
- Fully virtualized memory addressing for OS operation in a unified memory architecture
- Advanced and standard 2D operations [e.g., vector graphics, BLTs (block level transfers), ROPs (raster operations)] 32K stride support

SGX 3D Features

- Deferred pixel shading
- On-chip tile floating point depth buffer
- 8-bit stencil with on-chip tile stencil buffer
- 8 parallel depth/stencil tests per clock
- Scissor test
- Texture support:
 - Cube map
 - Projected textures
 - 2D textures
 - Non square textures
- Texture formats:
 - RGBA 8888, 565, 1555

- Monochromatic 8, 16, 16f, 32f, 32int
- Dual channel, 8:8, 16:16, 16f:16f
- Compressed textures PVR-TC1, PVR-TC2, ETC1
- Programmable support for all YUV formats
- Resolution support:
 - Frame buffer maximum size = 2048 x 2048
 - Texture maximum size = 2048 x 2048
- Texture filtering:
 - Bilinear, trilinear, anisotropic
 - Independent minimum and maximum control
- Antialiasing:
 - 4x multisampling
 - Up to 16x full scene anti-aliasing
 - Programmable sample positions
- Indexed primitive list support
 - Bus mastered
- Programmable vertex DMA
- Render to texture:
 - Including twiddled formats
 - Auto MipMap generation
- Multiple on-chip render targets (MRT).

2.1.3.5 Multichannel Audio Serial Port (McASP)

The Multichannel Audio Serial Port (McASP) functions as a general-purpose audio serial port optimized for the needs of multichannel audio applications. The McASP is useful for time-division multiplexed (TDM) stream, Inter-Integrated Sound (I2S) protocols, and inter-component digital audio interface transmission (DIT). The McASP consists of transmit and receive sections that may operate synchronized, or completely independently with separate master clocks, bit clocks, and frame syncs, and using different transmit modes with different bit-stream formats. The McASP module also includes serializers that can be individually enabled to either transmit or receive.

Features of the McASP include:

- Two independent clock generator modules for transmit and receive.
 - Clocking flexibility allows the McASP to receive and transmit at different rates. For example, the McASP can receive data at 48 kHz but output up-sampled data at 96 kHz or 192 kHz.
- Independent transmit and receive modules, each includes:
 - Programmable clock and frame sync generator.
 - TDM streams from 2 to 32, and 384 time slots.
 - Support for time slot sizes of 8, 12, 16, 20, 24, 28, and 32 bits.
 - Data formatter for bit manipulation.
- Individually assignable serial data pins (up to 6 pins).
- Glue less connection to audio analog-to-digital converters (ADC), digital-to-analog converters (DAC), codec, digital audio interface receiver (DIR), and S/PDIF transmit physical layer components.
- Wide variety of I2S and similar bit-stream format.

- Integrated digital audio interface transmitter (DIT) supports (up to 10 transmit pins):
 - S/PDIF, IEC60958-1, AES-3 formats.
 - Enhanced channel status/user data RAM.
- 384-slot TDM with external digital audio interface receiver (DIR) device.
 - For DIR reception, an external DIR receiver integrated circuit should be used with I2S output format and connected to the McASP receive section.
- Extensive error checking and recovery.
 - Transmit underruns and receiver overruns due to the system not meeting real-time requirements.
 - Early or late frame sync in TDM mode.
 - Out-of-range high-frequency master clock for both transmit and receive.
 - External error signal coming into the AMUTEIN input.
 - DMA error due to incorrect programming.

2.1.3.6 Ethernet Subsystem

The AM335x 3-port switch gigabit Ethernet subsystem provides Ethernet packet communication and can be configured as an Ethernet switch. It provides the Gigabit Media Independent Interface (GMII), Reduced Gigabit Media Independent Interface (RGMII), Reduced Media Independent Interface (RMII) and the Management Data Input Output (MDIO) for Physical-layer device (PHY) management.

The general features of the Ethernet switch subsystem are:

- Two 10/100/1000 Ethernet ports with MII, RMII and RGMII interfaces
- Wire rate switching (802.1d)
- Non Blocking switch fabric
- Flexible logical FIFO based packet buffer structure
- Four priority level QOS support (802.1p)
- CPPI 3.1 compliant DMA controllers
- Support for Audio/Video Bridging (P802.1Qav/D6.0)
- Support for IEEE 1588 Clock Synchronization (2008 Annex D and Annex F)
 - Timing FIFO and time stamping logic inside the SS
- Device Level Ring (DLR) Support
- Address Lookup Engine
 - 1024 addresses plus VLANs
 - Wire rate lookup
 - VLAN support
 - Host controlled time-based aging
 - Spanning tree support
 - L2 address lock and L2 filtering support
 - MAC authentication (802.1x)
 - Receive or destination based Multicast and Broadcast limits
 - MAC address blocking
 - Source port locking
 - OUI host accept/deny feature
- Flow Control Support (802.3x)
- EtherStats and 802.3Stats RMON statistics gathering (shared)

- Support for external packet dropping engine
- CPGMAC_SL transmit to CPGMAC_SL receive Loopback mode (digital loopback) supported
- CPGMAC_SL receive to CPGMAC_SL transmit Loopback mode (FIFO loopback) supported
- Maximum frame size 2016 bytes (2020 with VLAN)
- 8k (2048 x 32) internal CPPI buffer descriptor memory
- MDIO module for PHY Management
- Programmable interrupt control with selected interrupt pacing
- Emulation Support.
- Programmable transmit Inter-Packet Gap (IPG)
- Reset isolation

2.1.3.7 Universal Serial BUS

The USB controller provides a low-cost connectivity solution for numerous consumer portable devices by providing a mechanism for data transfer between USB devices with a line/bus speed up to 480 Mbps. The device USB subsystem has two independent USB 2.0 Modules built around two OTG controllers. The OTG supplement feature, the support for a dynamic role change, is also supported. Each port has the support for a dual-role feature allowing for additional versatility enabling operation capability as a host or peripheral. Both ports have identical capabilities and operate independent of each other.

The main features of the USB subsystem are:

- Contains 2 usb2otg_f controller modules with the following features:
 - Built around the Mentor USB 2.0 OTG core (musbmhdc)
 - Supports USB 2.0 peripheral at speeds HS (480 Mb/s) and FS (12 Mb/s)
 - Supports USB 2.0 host or OTG at speeds HS (480 Mb/s), FS (12 Mb/s), and LS (1.5 Mb/s)
 - Supports all modes of transfers (control, bulk, interrupt, and isochronous)
 - Supports high bandwidth ISO mode
 - Supports 16 Transmit (TX) and 16 Receive (RX) endpoints including endpoint 0
 - Supports USB OTG extensions for Session Resume (SRP) and Host Negotiation (HNP)
 - Includes a 32K endpoint FIFO RAM, and supports programmable FIFO sizes
 - Includes RNDIS mode for accelerating RNDIS type protocols using short packet termination over USB
 - Includes CDC Linux mode for accelerating CDC type protocols using short packet termination over USB
 - Includes an RNDIS like mode for terminating RNDIS type protocols without using short packet termination for support of MSC applications
- Includes 2 GS70 USB2.0 OTG PHYs in C014.M process
- Interfaces to the CPU via 3 OCP interfaces:
 - Master OCP HP interface for the DMA
 - Master OCP HP interface for the Queue manager
 - Slave OCP MMR interface
- Includes a CPPI 4.1 compliant DMA controller sub-module with 30 RX and 30 TX simultaneous data connections

- Includes a CPPI 4.1 DMA scheduler
- DMA supports CPPI host descriptor formats
- DMA supports stall on buffer starvation
- Supports data buffer sizes up to 4M bytes
- CPPI FIFO interface per TX/RX endpoint
- Provides a CPPI Queue Manager module with 92 queues for queuing/de-queuing packets.
- DMA pacing logic for interrupts
- Loopback MGC test using the UTMI interfaces

2.2 Memory

2.2.1 RAM

The VAR-SOM-AM33 is available with up to 4Gb of DDR3 memory.

2.2.2 Non-volatile Storage Memory

The VAR-SOM-AM33 is available with 2048 Mb of NAND FLASH memory. The NAND flash is used for flash disk purposes, O.S. run-time-image and the bootloader (boot from NAND). First block (block address 00h) of the memory device is guaranteed to be valid without ECC (up to 1,000 PROGRAM/ERASE cycles).

2.3 On-board Ethernet PHY

On-board, Micrel's KSZ8051RNL, is a single 10/100Base-Tx Ethernet physical layer transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair cable. KSZ8051RNL offers the Reduced Media Independent Interface (RMII) for direct connection with MII/RMII compliant Ethernet MAC processors and switches. Only magnetics and a RJ-45 connector are required on VAR-SOM-AM33 base board in order to have a fully functional 10/100Mbps Ethernet link.

2.4 TLV320AIC3106 Audio

The Texas Instrument's TLV320AIC3106 is a low-power, highly integrated stereo audio codec with stereo headphone amplifier, as well as multiple inputs and outputs programmable in single-ended or fully differential configurations. Extensive register-based power control is included, enabling stereo 48-kHz DAC playback as low as 15mW. VAR-SOM-AM33 exposes most of the audio interfaces of the TLV320AIC3106.

2.5 TPS65910 PMIC

The Texas Instrument's TPS65910 is an integrated power-management IC dedicated to applications processors as the AM335x. The device provides three step-down converters, one step-up converter, and eight LDOs and is designed to support the specific power requirements of OMAP-based applications.

Two of the step-down converters provide power for dual processor cores and are controllable by a dedicated class-3 SmartReflex interface for optimum power savings. The third converter provides power for the I/Os and memory in the system.

The eight general-purpose LDOs provide a wide range of voltage and current capabilities; they are fully controllable from the I2C interface. TPS65910 features are utilized internally by the VAR-SOM-AM33 and are not exposed to the VAR-SOM-AM33 200 pin connector

3 External Connectors

The VAR-SOM-AM33 exposes a 200-pin, SO-DIMM mechanical standard interface. The recommended mating connector for baseboard interfacing is FCI 10033853-052FSLF or equivalent. The following list describes this chapter's column header tables:

Pin#:

Pin Number on the SO-DIMM200 connector

Pin Name:

Default VAR- SOM-AM33 Pin Name

Type:

Pin Type & Direction:

- I – In
- O – Out
- DS – Differential Signal
- A – Analog
- Power – Power Pin

Pin Group:

Pin functionality group

AM335 Ball:

AM335x ball number

Mode (Tables 3.2 & 3.4):

AM335x PinMux mode option

3.1 SoM Connector Pin-out

Pin #	Pin Name	Type	Pin Group / Function	AM335 Ball
1	LCD_DATA11	I/O	LCD data B[3] / PinMux Table 3.2	U4
2	LCD_DATA12	I/O	LCD data B[4] / PinMux Table 3.2	V2
3	LCD_DATA13	I/O	LCD data B[5] / PinMux Table 3.2	V3
4	LCD_DATA14	I/O	LCD data B[6] / PinMux Table 3.2	V4
5	LCD_DATA15	I/O	LCD data B[7] / PinMux Table 3.2	T5
6	LCD_DATA5	I/O	LCD data G[2] / PinMux Table 3.2	T2
7	DGND	Power	Digital GND	
8	DGND	Power	Digital GND	
9	LCD_DATA6	I/O	LCD data G[3] / PinMux Table 3.2	T3
10	LCD_DATA7	I/O	LCD data G[4] / PinMux Table 3.2	T4
11	LCD_DATA8	I/O	LCD data G[5] / PinMux Table 3.2	U1
12	LCD_DATA9	I/O	LCD data G[6] / PinMux Table 3.2	U2

Pin #	Pin Name	Type	Pin Group / Function	AM335 Ball
13	LCD_DATA10	I/O	LCD data G[7] / PinMux Table 3.2	U3
14	LCD_DATA1	I/O	LCD data R[4] / PinMux Table 3.2	R2
15	LCD_DATA0	I/O	LCD data R[3] / PinMux Table 3.2	R1
16	LCD_DATA3	I/O	LCD data R[6] / PinMux Table 3.2	R4
17	LCD_DATA2	I/O	LCD data R[5] / PinMux Table 3.2	R3
18	DGND	Power	Digital GND	
19	LCD_DATA4	I/O	LCD data R[7] / PinMux Table 3.2	T1
20	LCD_HSYNC	O	LCD horizontal sync / PinMux Table 3.2	R5
21	LCD_AC_BIAS_EN	O	LCD AC bias enable / PinMux Table 3.2	R6
22	LCD_PCLK	O	LCD pixel clock / PinMux Table 3.2	V5
23	DGND	Power	Digital GND	
24	LCD_VSYNC	O	LCD vertical sync / PinMux Table 3.2	U5
25	AIN3	A	Touch screen Y minus / analog I	A7
26	DGND	Power	Digital GND	
27	AIN2	A	Touch screen X minus / analog I	B7
28	AIN0	A	Touch screen X plus / analog I	B6
29	AIN6	A	Analog input	A8
30	AIN1	A	Touch screen Y plus / analog I	C7
31	AIN7	A	Analog input	C9
32	AIN4	A	Analog input	C8
33	DGND	Power	Digital GND	
34	AIN5	A	Analog input	B8
35	UART0_RX	I	UART receive data / PinMux Table 3.2	E15
36	DGND	Power	Digital GND	
37	UART0_TX	O	UART Transmit Data / PinMux Table 3.2	E16
38	JTAG_TDI	I	JTAG data input	B11
39	JTAG_TRSTN	I	TEST reset (active low)	B10
40	JTAG_TMS	I	JTAG test mode select	C11
41	JTAG_TDO	O	JTAG data out	A11
42	DGND	Power	Digital GND	
43	JTAG_TCK	I	JTAG clock	A12
44	GPMC_A0	O	GPMC address / PinMux Table 3.2	R13
45	DGND	Power	Digital GND	
46	GPMC_A2	O	GPMC address / PinMux Table 3.2	U14
47	GPMC_CSN3	O	GPMC chip select / PinMux Table 3.2	T13
48	GPMC_A4	O	GPMC address / PinMux Table 3.2	R14
49	GPMC_A1	O	GPMC address / PinMux Table 3.2	V14
50	GPMC_A6	O	GPMC address / PinMux Table 3.2	U15
51	GPMC_A3	O	GPMC address / PinMux Table 3.2	T14
52	DGND	Power	Digital GND	

Pin #	Pin Name	Type	Pin Group / Function	AM335 Ball
53	GPMC_A5	O	GPMC address / PinMux Table 3.2	V15
54	GPMC_A8	O	GPMC address / PinMux Table 3.2	V16
55	GPMC_A7	O	GPMC address / PinMux Table 3.2	T15
56	GPMC_A10	O	GPMC address / PinMux Table 3.2	T16
57	DGND	Power	Digital GND	
58	GPMC_BE1N	O	GPMC byte enable 1 / PinMux Table 3.2	U18
59	GPMC_A9	O	GPMC address / PinMux Table 3.2	U16
60	GPMC_WPN	O	GPMC write protect	U17
61	GPMC_A11	O	GPMC address / PinMux Table 3.2	V17
62	USB1_ID	I	USB1 OTG ID	P17
63	GPMC_WAIT0	I	GPMC wait0	T17
64	USB1_VBUS	I	USB OTG VBUS	T18
65	USB1_DP	I/ODS	USB OTG data pair, positive line	R17
66	GPIO2_18	I/O	PinMux Table 3.2	L17
67	USB1_DM	I/ODS	USB OTG data pair, negative line	R18
68	NC			
69	DGND	Power	Digital GND	
70	GPIO3_10	I/O	PinMux Table 3.2	L18
71	USB0_DP	I/ODS	USB host data pair, positive line	N17
72	GPIO3_9	I/O	PinMux Table 3.2	K18
73	USB0_DM	I/ODS	USB host data pair, negative line	N18
74	USB0_VBUS	I	USB host VBUS	P15
75	DGND	Power	Digital GND	
76	GPMC_CLK	O	GPMC clock / PinMux Table 3.2	V12
77	GPMC_AD1	I/O	GPMC - Local Bus	V7
78	GPMC_AD0	I/O	GPMC - Local Bus	U7
79	GPMC_AD3	I/O	GPMC - Local Bus	T8
80	GPMC_AD2	I/O	GPMC - Local Bus	R8
81	GPMC_AD5	I/O	GPMC - Local Bus	V8
82	GPMC_AD4	I/O	GPMC - Local Bus	U8
83	GPMC_AD7	I/O	GPMC - Local Bus	T9
84	GPMC_AD6	I/O	GPMC - Local Bus	R9
85	GPMC_AD13	I/O	GPMC - Local Bus/ PinMux Table 3.2	R12
86	GPMC_AD12	I/O	GPMC - Local Bus/ PinMux Table 3.2	T12
87	GPMC_AD15	I/O	GPMC - Local Bus/ PinMux Table 3.2	U13
88	GPMC_AD14	I/O	GPMC - Local Bus/ PinMux Table 3.2	V13
89	DGND	Power	Digital GND	
90	DGND	Power	Digital GND	
91	DCAN0_RX	I	DCAN0 receive data / PinMux Table 3.2	K15

Pin #	Pin Name	Type	Pin Group / Function	AM335 Ball
92	MDIO_CLK	O	MDIO clock/ PinMux Table 3.2	M18
93	DCAN0_TX	O	DCAN0 transmit data / PinMux Table 3.2	J18
94	MDIO_DATA	I/O	MDIO data / PinMux Table 3.2	M17
95	DGND	Power	Digital GND	
96	DGND	Power	Digital GND	
97	MMC0_DAT0	I/O	MMC/SD/SDIO data bus / PinMux Table 3.2	G16
98	MMC0_DAT2	I/O	MMC/SD/SDIO data bus / PinMux Table 3.2	F18
99	MMC0_DAT1	I/O	MMC/SD/SDIO data bus / PinMux Table 3.2	G15
100	MMC0_DAT3	I/O	MMC/SD/SDIO data bus / PinMux Table 3.2	F17
101	MMC0_CMD	I/O	MMC/SD/SDIO command / PinMux Table 3.2	G18
102	DGND	Power	Digital GND	
103	MMC0_CLKO		MMC/SD/SDIO clock	G17
104	I2C1_SDA	I/OD	I2C1 data / PinMux Table 3.2	B16
105	DGND	Power	Digital GND	
106	I2C1_SCL	I/OD	I2C1 clock / PinMux Table 3.2	A16
107	NC			
108	NC			
109	WAKEUP	I	AM335x WAKEUP pin - TBD	C5
110	NC			
111	GPIO_3_7	I/O	PinMux Table 3.2	C14
112	NC			
113	NC			
114	ETH_RXDN	IDS	Ethernet PHY, Rx negative	
115	LINKLED	O	Link activity indication	
116	ETH_RXDP	IDS	Ethernet PHY, Rx positive	
117	LINKSPEED	O	Ethernet PHY, link speed indication	
118	ETH_TXDN	ODS	Ethernet PHY, Tx negative	
119	NC			
120	ETH_TXDP	ODS	Ethernet PHY, Tx positive	
121	NC			
122	DGND	Power	Digital GND	
123	DGND	Power	Digital GND	
124	NC			
125	DGND	Power	Digital GND	
126	PB_POWERON	I	PMIC push button power on pin - TBD	
127	NC			

Pin #	Pin Name	Type	Pin Group / Function	AM335 Ball
128	PMIC_PWR_EN	O	Internally used for PMIC enable	C6
129	SYS_RESETn	I	Reset in, active low	A10
130	DGND	Power	Digital GND	
131	DGND	Power	Digital GND	
132	VIN	Power	Digital power	
133	DGND	Power	Digital GND	
134	VIN	Power	Digital power	
135	NC			
136	VIN	Power	Digital power	
137	NC			
138	VIN	Power	Digital power	
139	NC			
140	VIN	Power	Digital power	
141	NC			
142	VIN	Power	Digital power	
143	DGND	Power	Digital GND	
144	VIN	Power		
145	DGND	Power	Digital GND	
146	NC			
147	NC			
148	GPMC_AD11_MMC1_DAT3	I/O	GPMC - Local Bus/ PinMux Table 3.2 ^[1]	U12
149	MMC1_CMD	I/O	MMC/SD/SDIO command / PinMux Table 3.2	V9
150	GPMC_AD10_MMC1_DAT2	I/O	GPMC - Local Bus/ PinMux Table 3.2 ^[1]	T11
151	MMC1_CLK	I/O	MMC/SD/SDIO clock	U9
152	GPMC_AD9_MMC1_DAT1	I/O	GPMC - Local Bus/ PinMux Table 3.2 ^[1]	T10
153	UART1_CTSN	I	UART1 clear to send / PinMux Table 3.2	D18
154	GPMC_AD8_MMC1_DAT0	I/O	GPMC - Local Bus/ PinMux Table 3.2 ^[1]	U10
155	UART1_RTSN	O	UART1 request to send / PinMux Table 3.2	D17
156	UART1_RXD	I	UART1 receive data / PinMux Table 3.2	D16
157	GPIO_0_3	I/O	PinMux Table 3.2	B17
158	UART1_TXD	O	UART transmit data / PinMux Table 3.2	D15
159	EHRPWM0A	O	PWM0 A output / PinMux Table 3.2	A17
160	GPIO_3_8	I/O	PinMux Table 3.2	B14
161	SPI1_CS0	I/O	SPI chip select / PinMux Table 3.2	C12
162	GPMC_OEN_REN	O	GPMC output / read enable	T7

Pin #	Pin Name	Type	Pin Group / Function	AM335 Ball
163	SPI1_D0	I/O	SPI1 data 0 / PinMux Table 3.2	E18
164	GPMC_WEN	O	GPMC write enable	U6
165	SPI1_D1	I/O	SPI data 1/ PinMux Table 3.2	E17
166	GPMC_ADV_N_ALE	O	GPMC address valid / address latch enable	R7
167	SPI1_SCLK	I/O	SPI clock / PinMux Table 3.2	H16
168	GPMC_BE0N_CLE	O	GPMC byte enable 0	T6
169	VBCKUPBAT	Power	RTC backup battery input	
170	VCC_3V3	Power	Digital signal IO level	E10
171	UART3_RXD	I	UART receive data / PinMux Table 3.2	C15
172	I2C0_SCL	I/O	I2C0 clock ^[2]	C16
173	UART3_TXD	O	UART transmit data / PinMux Table 3.2	C18
174	I2C0_SDA	I/O	I2C0 data ^[2]	C17
175	DMIC_DATA	I	Digital microphone data	
176	DMIC_CLK	O	Digital microphone clock	
177	AGND	Power		
178	AGND	Power		
179	LINEIN1_RP	A	MIC1 or line1 analog input (right + or multifunction)	
180	LINEIN1_LP	A	MIC1 or line1 analog input (left + or multifunction)	
181	LINEIN1_RM	A	MIC1 or line1 analog input (right – or multifunction)	
182	LINEIN1_LM	A	MIC1 or line1 analog input (left – or multifunction)	
183	LINEIN2_LP	A	MIC2 or line2 analog input (left + or multifunction)	
184	LINEIN2_RM	A	MIC1 or line1 analog input (right – or multifunction)	
185	LINEIN2_LM	A	MIC2 or line2 analog input (left – or multifunction)	
186	LINEIN2_RP	A	MIC2 or line2 analog input (right + or multifunction)	
187	LINEOUT_LM	A	Left line output (–)	
188	AGND	Power	Audio GND	
189	LINEOUT_LP	A	Left line output (+)	
190	HPLOUT	A	High-power output driver (left +)	
191	LINEOUT_RM	A	Right line output (–)	
192	HPROUT	A	High-power output driver (right +)	
193	LINEOUT_RP	A	Right line output (+)	
194	AGND	Power	Audio GND	
195	AGND	Power	Audio GND	
196	MICBIAS	A	Microphone bias voltage output	

Pin #	Pin Name	Type	Pin Group / Function	AM335 Ball
197	MIC_IN_R	A	MIC input (right)	
198	MIC_IN_L	A	MIC input (left)	
199	AGND	Power	Audio GND	
200	AGND	Power	Audio GND	

Table 3-1 SO-DIMM200 Pin Out

Notes:

[1] Do not use when on-board Wi-Fi module is being used

[2] I2C0 is internally used by PMIC (0x12h, 0x2Dh) and AUDIO IC (0x1Bh)

3.2 SO-DIMM 200 Pin Mux

The table below summarizes the additional available functionality for each SO-DIMM 200 connector. Default pin mode is marked in bold.

Pin #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
1	LCD_DATA11	GPMC_A15	EHRPWM1B	MCASP0_AHCLKR	MCASP0_AXR2	PR1_MII0_RXD0	GPIO2_17	UART3_RT SN
2	LCD_DATA12	GPMC_A16	EQEP1A_IN	MCASP0_ACLKR	MCASP0_AXR2	PR1_MII0_RXLINK	GPIO0_8	UART4_CT SN
3	LCD_DATA13	GPMC_A17	EQEP1B_IN	MCASP0_FSR	MCASP0_AXR3	PR1_MII0_RXER	GPIO0_9	UART4_RT SN
4	LCD_DATA14	GPMC_A18	EQEP1_INDEX	MCASP0_AXR1	UART5_RXD	PR1_MII_MR0_CLK	GPIO0_10	UART5_CT SN
5	LCD_DATA15	GPMC_A19	EQEP1_STROBE	MCASP0_AHCLKX	MCASP0_AXR3	PR1_MII0_RXDV	GPIO0_11	UART5_RT SN
6	LCD_DATA5	GPMC_A5		EQEP2B_IN		PR1_PRU1_PRU_R30_5	GPIO2_11	PR1_PRU1_PRU_R31_5
9	LCD_DATA6	GPMC_A6	PR1_EDIO_DATA_IN6	EQEP2_INDEX	PR1_EDIO_DATA_OUT6	PR1_PRU1_PRU_R30_6	GPIO2_12	PR1_PRU1_PRU_R31_6
10	LCD_DATA7	GPMC_A7	PR1_EDIO_DATA_IN7	EQEP2_STROBE	PR1_EDIO_DATA_OUT7	PR1_PRU1_PRU_R30_7	GPIO2_13	PR1_PRU1_PRU_R31_7
11	LCD_DATA8	GPMC_A12	EHRPWM1_TRIPZONE_INPUT	MCASP0_ACLKX	UART5_TXD	PR1_MII0_RXD3	GPIO2_14	UART2_CT SN
12	LCD_DATA9	GPMC_A13	EHRPWM1_SYNCI_O	MCASP0_FSX	UART5_RXD	PR1_MII0_RXD2	GPIO2_15	UART2_RT SN
13	LCD_DATA10	GPMC_A14	EHRPWM1A	MCASP0_AXR0		PR1_MII0_RXD1	GPIO2_16	UART3_CT SN
14	LCD_DATA1	GPMC_A1		EHRPWM2B		PR1_PRU1_PRU_R30_1	GPIO2_7	PR1_PRU1_PRU_R31_1
15	LCD_DATA0	GPMC_A0		EHRPWM2A		PR1_PRU1_PRU_R30_0	GPIO2_6	PR1_PRU1_PRU_R31_0
16	LCD_DATA3	GPMC_A3		EHRPWM2_SYNCI_O		PR1_PRU1_PRU_R30_3	GPIO2_9	PR1_PRU1_PRU_R31_3
17	LCD_DATA2	GPMC_A2		EHRPWM2_TRIPZONE_INPUT		PR1_PRU1_PRU_R30_2	GPIO2_8	PR1_PRU1_PRU_R31_2
19	LCD_DATA4	GPMC_A4		EQEP2A_IN		PR1_PRU1_PRU_R30_4	GPIO2_10	PR1_PRU1_PRU_R31_4
20	LCD_HSYNC	GPMC_A9		PR1_EDIO_DATA_IN3	PR1_EDIO_DATA_OUT3	PR1_PRU1_PRU_R30_9	GPIO2_23	PR1_PRU1_PRU_R31_9
21	LCD_AC_BIAS_EN	GPMC_A11		PR1_EDIO_DATA_IN5	PR1_EDIO_DATA_OUT5	PR1_PRU1_PRU_R30_11	GPIO2_25	PR1_PRU1_PRU_R31_11
22	LCD_PCLK	GPMC_A10	PR1_MII0_CRC	PR1_EDIO_DATA_IN4	PR1_EDIO_DATA_OUT4	PR1_PRU1_PRU_R30_10	GPIO2_24	PR1_PRU1_PRU_R31_10
24	LCD_VSYNC	GPMC_A8		PR1_EDIO_DATA_IN2	PR1_EDIO_DATA_OUT2	PR1_PRU1_PRU_R30_8	GPIO2_22	PR1_PRU1_PRU_R31_8
35	UART0_RXD	SPI1_CS0	DCAN0_TX	I2C2_SDA	ECAP2_IN_PWM2_OUT	PR1_PRU1_PRU_R30_14	GPIO1_10	PR1_PRU1_PRU_R31_14
37	UART0_TXD	SPI1_CS1	DCAN0_RX	I2C2_SCL	ECAP1_IN_PWM1_OUT	PR1_PRU1_PRU_R30_15	GPIO1_11	PR1_PRU1_PRU_R31_15
44	GPMC_A0	GMII2_TXEN	RGMII2_TCTL	RMII2_TXEN	GPMC_A16	PR1_MII_MT1_CLK	GPIO1_16	EHRPWM1_TRIPZONE_INPUT
46	GPMC_A2	GMII2_TXD3	RGMII2_TD3	MMC2_DAT1	GPMC_A18	PR1_MII1_TXD2	GPIO1_18	EHRPWM1A
47	GPMC_CSN3	MMC2_CMD	PR1_MDIO_DATA	GPIO2_0	PR1_MII0_CRS	PR1_MDIO_DATA		
48	GPMC_A4	GMII2_TXD1	RGMII2_TD1	RMII2_TXD1	GPMC_A20	PR1_MII1_TXD0	GPIO1_20	EQEP1A_IN
49	GPMC_A1	GMII2_RXDV	RGMII2_RCTL	MMC2_DAT0	GPMC_A17	PR1_MII1_TXD3	GPIO1_17	EHRPWM1_SYNCI_O

VAR-SOM-AM33 SYSTEM ON MODULE

Pin #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
50	GPMC_A6	GMII2_TXCLK	RGMII2_TCLK	MMC2_DAT4	GPMC_A22	PR1_MII1_RX D2	GPIO1_22	EQEP1_IND EX
51	GPMC_A3	GMII2_TXD2	RGMII2_TD2	MMC2_DAT2	GPMC_A19	PR1_MII1_TX D1	GPIO1_19	EHRPWM1 B
53	GPMC_A5	GMII2_TXD0	RGMII2_TD0	RMII2_TXD0	GPMC_A21	PR1_MII1_RX D3	GPIO1_21	EQEP1B_IN
54	GPMC_A8	GMII2_RXD3	RGMII2_RD3	MMC2_DAT6	GPMC_A24	PR1_MII1_RX D0	GPIO1_24	MCASP0_A CLKX
55	GPMC_A7	GMII2_RXCLK	RGMII2_RCLK	MMC2_DAT5	GPMC_A23	PR1_MII1_RX D1	GPIO1_23	EQEP1_ST ROBE
56	GPMC_A10	GMII2_RXD1	RGMII2_RD1	RMII2_RXD1	GPMC_A26	PR1_MII1_RX DV	GPIO1_26	MCASP0_A XR0
58	GPMC_BE1N	GMII2_COL	GPMC_CSN6	MMC2_DAT3	GPMC_DIR	PR1_MII1_RX LINK	GPIO1_28	MCASP0_A CLKR
59	GPMC_A9	GMII2_RXD2	RGMII2_RD2	MMC2_DAT7	GPMC_A25	PR1_MII1_MR1_CLK	GPIO1_25	MCASP0_F SX
61	GPMC_A11	GMII2_RXD0	RGMII2_RD0	RMII2_RXD0	GPMC_A27	PR1_MII1_RX ER	GPIO1_27	MCASP0_A XR1
66	GMII1_RXD3	UART3_RXD	RGMII1_RD3	MMC0_DAT5	MMC1_DAT2	UART1_DTRN	GPIO2_18	MCASP0_A XR0
70	GMII1_RXCLK	UART2_TXD	RGMII1_RCLK	MMC0_DAT6	MMC1_DAT1	UART1_DSRN	GPIO3_10	MCASP0_F SX
72	GMII1_TXCLK	UART2_RXD	RGMII1_TCLK	MMC0_DAT7	MMC1_DAT0	UART1_DCDN	GPIO3_9	MCASP0_A CLKX
76	GPMC_CLK	LCD_MEM_CLK	GPMC_WAIT1	MMC2_CLK	PRT1_MII1_CRS	PR1_MII1_md clk	GPIO2_1	MCASP0_F SR
85	GPMC_AD13	LCD_DATA18	MMC1_DAT5	MMC2_DAT1	EQEP2B_IN	PR1_MII0_TX D1	GPIO1_13	PR1_PRU0_P RU_R30_15
86	GPMC_AD12	LCD_DATA19	MMC1_DAT4	MMC2_DAT0	EQEP2A_IN	PR1_MII0_TX D2	GPIO1_12	PR1_PRU0_P RU_R30_14
87	GPMC_AD15	LCD_DATA16	MMC1_DAT7	MMC2_DAT3	EQEP2_STRO BE	PR1_ECAP0_ECAP_CAPIN_APWM_O	GPIO1_15	PR1_PRU0_P RU_R31_15
88	GPMC_AD14	LCD_DATA17	MMC1_DAT6	MMC2_DAT2	EQEP2_INDEX	PR1_MII0_TX D0	GPIO1_14	PR1_PRU0_P RU_R31_14
91	GMII1_TXD2	DCAN0_RX	RGMII1_TD2	UART4_TXD	MCASP1_AXR0	MMC2_DAT2	GPIO0_17	MCASP0_A HCLKX
92	MDIO_CLK	TIMER5	UART5_TXD	UART3_RTSN	MMC0_SDWP	MMC1_CLK	GPIO0_1	MMC2_CLK
93	GMII1_TXD3	DCAN0_TX	RGMII1_TD3	UART4_RXD	MCASP1_FSX	MMC2_DAT1	GPIO0_16	MCASP0_F SR
94	MDIO_DATA	TIMER6	UART5_RXD	UART3_CTSN	MMC0_SDCD	MMC1_CMD	GPIO0_0	MMC2_CM D
97	MMC0_DAT0	GPMC_A23	UART5_RTSN	UART3_TXD	UART1_RIN	PR1_PRU0_P RU_R30_11	GPIO2_29	PR1_PRU0_P RU_R31_11
98	MMC0_DAT2	GPMC_A21	UART4_RTSN	TIMER6	UART1_DSRN	PR1_PRU0_P RU_R30_9	GPIO2_27	PR1_PRU0_P RU_R31_9
99	MMC0_DAT1	GPMC_A22	UART5_CTSN	UART3_RXD	UART1_DTRN	PR1_PRU0_P RU_R30_10	GPIO2_28	PR1_PRU0_P RU_R31_10
100	MMC0_DAT3	GPMC_A20	UART4_CTSN	TIMER5	UART1_DCDN	PR1_PRU0_P RU_R30_8	GPIO2_26	PR1_PRU0_P RU_R31_8
101	MMC0_CMD	GPMC_A25	UART3_RTSN	UART2_TXD	DCAN1_RX	PR1_PRU0_P RU_R30_13	GPIO2_31	PR1_PRU0_P RU_R31_13
103	MMC0_CLK	GPMC_A24	UART3_CTSN	UART2_RXD	DCAN1_TX	PR1_PRU0_P RU_R30_12	GPIO2_30	PR1_PRU0_P RU_R31_12
104	SPI0_D1	MMC1_SDWP	I2C1_SDA	EHRPWM0_TRI PZONE_INPUT	PR1_UART0_RXD	PR1_EDIO_D ATA_IN0	GPIO0_4	PR1_EDIO_DATA_OUT 0
106	SPI0_CS0	MMC2_SDWP	I2C1_SCL	EHRPWM0_SY NCI_O	PR1_UART0_TXD	PR1_EDIO_D ATA_IN1	GPIO0_5	PR1_EDIO_DATA_OUT 1
111	EMU0	GPIO3_7						
148	GPMC_AD11	LCD_DATA20	MMC1_DAT3	MMC2_DAT7	EHRPWM2_SY NCI_O	PR1_MII0_TX D3	GPIO0_27	
149	GPMC_CSN2	GPMC_BE1N	MMC1_CMD	PR1_EDIO_DAT	PR1_EDIO_DA	PR1_PRU1_P	GPIO1_31	PR1_PRU1_

VAR-SOM-AM33 SYSTEM ON MODULE

				A_IN7	TA_OUT7	RU_R30_13		PRU_R31_13
150	GPMC_AD10	LCD_DATA21	MMC1_DAT2	MMC2_DAT6	EHRPWM2_TRIPZONE_INPUT	PR1_MII0_TXEN	GPIO0_26	
151	GPMC_CSN1	GPMC_CLK	MMC1_CLK	PRT1EDIO_DATA_IN6	PRT1_EDIO_DATA_OUT6	PR1_PRU1_PRU_R30_12	GPIO1_30	
152	GPMC_AD9	LCD_DATA22	MMC1_DAT1	MMC2_DAT5	EHRPWM2B	PR1_MII0_COLL	GPIO0_23	
153	UART1_CTSN	TIMER6	DCAN0_TX	I2C2_SDA	SPI1_CS0	PR1_UART0_CTS_N	GPIO0_12	PR1_EDC_LATCH0_IN
154	GPMC_AD8	LCD_DATA23	MMC1_DAT0	MMC2_DAT4	EHRPWM2A	PR1_MII_MT0_CLK	GPIO0_22	
155	UART1_RTSN	TIMER5	DCAN0_RX	I2C2_SCL	SPI1_CS1	PR1_UART0_RTS_N	GPIO0_13	PR1_EDC_LATCH1_IN
156	UART1_RXD	MMC2_SDWP	DCAN1_TX	I2C1_SDA		PR1_UART0_RXD	GPIO0_14	PR1_PRU1_PRU_R31_16
157	SPI0_D0	UART2_TXD	I2C2_SCL	EHRPWM0B	PR1_UART0_RTS_N	PR1_EDIO_LATCH_IN	GPIO0_3	EMU3
158	UART1_TXD	MMC2_SDWP	DCAN1_RX	I2C1_SCL		PR1_UART0_TXD	GPIO0_15	PR1_PRU0_PRU_R31_16
159	SPI0_SCLK	UART2_RXD	I2C2_SDA	EHRPWM0A	PR1_UART0_CTS_N	PR1_EDIO_SOFT	GPIO0_2	EMU2
160	EMU1	GPIO3_8						
161	MCASP0_AHCLKR	EHRPWM0_SYNCI_O	MCASP0_AXR2	SPI1_CS0	ECAP2_IN_PWM2_OUT	PR1_PRU0_PRU_R30_3	GPIO3_17	PR1_PRU0_PRU_R31_3
163	UART0_CTSN	UART4_RXD	DCAN1_TX	I2C1_SDA	SPI1_D0	TIMER7	GPIO1_8	PR1_EDC_SYNC0_OUTPUT
165	UART0_RTSN	UART4_TXD	DCAN1_RX	I2C1_SCL	SPI1_D1	SPI1_CS0	GPIO1_9	PR1_EDC_SYNC1_OUTPUT
167	GMII1_COL	RMII2_REFCLK	SPI1_SCLK	UART5_RXD	MCASP1_AXR2	MMC2_DAT3	GPIO3_0	MCASP0_AXR2
171	SPI0_CS1	UART3_RXD	ECAP1_IN_PWM1_OUT	MMC0_POW	XDMA_EVENT_INTR2	MMC0_SDCD	GPIO0_6	EMU4
173	ECAP0_IN_PWM0_OUT	UART3_TXD	SPI1_CS1	PR1_ECAP0_ECAP_CAPIN_A_PWM_O	SPI1_SCLK	MMC0_SDWP	GPIO0_7	XDMA_EVENT_INTR2

Table 3-2 SO-DIMM 200 Pin MuX

4 Interface Details

4.1 Overview

This chapter describes in detail the VAR-SOM-AM33 interfaces, referring to the default SoM pin names. However, many additional interfaces are available when different pin modes are selected by the user. For example, the LSB of the LCD interface is available to the user when some GPMC pins modes are set to '1'. [PinMux Table 3.2](#) details the additional possible options for each pin on the VAR-SOM-AM33 connectors.

The following list describes this chapter's column header tables:

Signal:

VAR-SOM-AM33 original pin name

Pin#:

Pin Number on the SO-DIMM200 connector

Type:

Pin Type & Direction:

- I – In
- O – Out
- DS – Differential Signal
- A – Analog
- Power – Power Pin

Description:

Short Pin functionality description

4.2 Display Interfaces

The VAR-SOM-AM33 provides the logic to display a video frame from the memory frame buffer on a LCD panel using an up to 24-bit parallel RGB bus.

LCD interface signals are directly driven by the AM335x device, refer to [LCD controller](#) section in Chapter 2 for more details.

4.2.1.1 Signals

Signal	Pin #	Type	Description
LCD_DATA11	1	O	LCD data B[3]
LCD_DATA12	2	O	LCD data B[4]
LCD_DATA13	3	O	LCD data B[5]
LCD_DATA14	4	O	LCD data B[6]
LCD_DATA15	5	O	LCD data B[7]
LCD_DATA5	6	O	LCD data G[2]
LCD_DATA6	9	O	LCD data G[3]
LCD_DATA7	10	O	LCD data G[4]
LCD_DATA8	11	O	LCD data G[5]
LCD_DATA9	12	O	LCD data G[6]
LCD_DATA10	13	O	LCD data G[7]

Signal	Pin #	Type	Description
LCD_DATA1	14	O	LCD data R[4]
LCD_DATA0	15	O	LCD data R[3]
LCD_DATA3	16	O	LCD data R[6]
LCD_DATA2	17	O	LCD data R[5]
LCD_DATA4	19	O	LCD data R[7]
LCD_HSYNC	20	O	LCD horizontal sync
LCD_AC_BIAS_EN	21	O	LCD AC bias enable CS
LCD_PCLK	22	O	LCD pixel clock
LCD_VSYNC	24	O	LCD vertical sync

Table 4-1 Display Signals

4.3 Ethernet

4.3.1 10/100 Base-T Interface

The Ethernet interface is based on AM335x internal Ethernet MAC and an on board KSZ8051RNL PHY. Refer to [Ethernet Subsystem](#) section in Chapter 2 for Ethernet MAC details

4.3.2 Ethernet PHY Features

- 10BASE-T, 100BASE-TX , compliant with IEEE802.3/802.3u/802.3ab
- HP Auto MDI/MDI-X for reliable detection and correction for straight-through and crossover cables with disable and enable option
- Auto-negotiation to automatically select the highest link-up speed (10/100 Mbps) and duplex (half/full)
- LinkMD® TDR based cable diagnostics for identification of faulty copper cabling
- Back-to-back mode support for 100 Mbps copper repeater or media converter
- Programmable interrupt output
- Power down and power saving modes
- Baseline wander correction

Signal	Pin #	Type	Description
ETH_RXDN	114	IDS	Ethernet PHY differential receive negative
ETH_RXDP	116	IDS	Ethernet PHY differential receive positive
ETH_TXDN	118	ODS	Ethernet PHY differential transmit negative
ETH_TXDP	120	ODS	Ethernet PHY differential transmit positive
LINK_LED	115	O	Activity indicator
LINK_SPEED	117	O	Speed indicator

Table 4-2 Ethernet Signals

4.3.3 Gigabit Ethernet

Additional Ethernet MAC, supporting up to 1000 Mbps Ethernet link is supported by using RGMII & MDIO interfaces. The RGMII interface is available by setting pin mode2 for the relevant pins.

4.3.4 RGMII Signals

Signal	Pin #	Type	Description
RGMII2_RCLK	55	I	Receive reference clock
RGMII2_RCTL	49	I	Receive control
RGMII2_RD0	61	I	RGMII receive data 0
RGMII2_RD1	56	I	RGMII receive data 1
RGMII2_RD2	59	I	RGMII receive data 2
RGMII2_RD3	54	I	RGMII receive data 3
RGMII2_TCLK	50	O	Transmit reference clock
RGMII2_TCTL	44	O	Transmit control
RGMII2_TD0	53	O	RGMII transmit data 0
RGMII2_TD1	48	O	RGMII transmit data 1
RGMII2_TD2	51	O	RGMII transmit data 2
RGMII2_TD3	46	O	RGMII transmit data 3

Table 4-3 Ethernet Signals

4.4 USB HOST 2.0

USB host interface is based on the AM335x Universal Serial Bus controller, internally configured as USB HOST. Refer to [Universal Serial Bus controller](#) section in Chapter 2 for USB interface details.

4.4.1 USB Host Signals

Signal	Pin #	Type	Description
USB0_DP	71	I/ODS	USB host data negative
USB0_DM	73	I/ODS	USB host data positive
USB0_VBUS	74	I	

Table 4-4 USB Host1 Signals

4.5 USB 2.0 On-the-Go

USB host interface is based on the AM335x Universal Serial Bus controller. Refer to the [Universal Serial Bus controller](#) section in Chapter 2 for USB interface details.

4.5.1 OTG Signals

Signal	Pin #	Type	Description
USB1_ID	62	I	USB OTG ID
USB1_VBUS	64	I	USB OTG VBUS
USB1_DP	65	I/ODS	USB OTG data positive
USB1_DM	67	I/ODS	USB OTG data negative

Table 4-5 USB OTG Signals

4.6 MMC/SD/SDIO

This device contains two MultiMedia Card (MMC), Secure Digital (SD), and Secure Digital I/O (SDIO) high speed interface module (MMCHS). The controller provides an interface to an MMC, SD memory card or SDIO card.

4.6.1 MMC/SD/SDIO Features

The general features of the MMCHS host controller IP are:

- Built-in 1024-byte buffer for read or write
- Two DMA channels, one interrupt line
- Clock support
 - 96-MHz functional clock source input
 - up to 192 Mbit/sec (24 MByte/sec) in High-Speed SD mode 4-bit data transfer
 - up to 24 Mbit/sec (3 MByte/sec) in default SD mode 1-bit data transfer
- Support for SDA 3.0 Part A2 programming model
- Serial link supports full compliance with:

- MMC command/response sets as defined in the MMC standard specification v4.3
- SD command/response sets as defined in the SD physical layer specification v3.00
- SDIO command/response sets and interrupt/read-wait suspend-resume operations as defined in the SD part E1 specification v 2 .00
- SD Host Controller Standard Specification sets as defined in the SD card specification Part A2 v2.00

4.6.2 SDMMC0 Signals

Signal	Pin #	Type	Description
MMC0_CLKO	103	O	MMC/SD/SDIO clock
MMC0_CMD	101	I/O	MMC/SD/SDIO command
MMC0_DAT0	97	I/O	MMC/SD/SDIO data 0
MMC0_DAT1	99	I/O	MMC/SD/SDIO data 1
MMC0_DAT2	98	I/O	MMC/SD/SDIO data 2
MMC0_DAT3	100	I/O	MMC/SD/SDIO data 3

Table 4-6 SDMMC0 Signals

4.6.3 SDMMC1 Signals

Signal	Pin #	Type	Description
MMC1_CLKO	151	I/O	MMC/SD/SDIO clock
MMC1_CMD	149	I/O	MMC/SD/SDIO command
MMC1_DAT0	154	I/O	MMC/SD/SDIO data 0
MMC1_DAT1	152	I/O	MMC/SD/SDIO data 1
MMC1_DAT2	150	I/O	MMC/SD/SDIO data 2
MMC1_DAT3	148	I/O	MMC/SD/SDIO data 3

Table 4-7 SDMMC1 Signals

Note: MMC1 signals are shared with the on board Wi-Fi module

4.7 Audio

4.7.1 Audio CODEC

Audio interfaces are featured by an on-board Texas Instrument's feature-rich [TLV320AIC3106](#) audio codec device. Please refer to the [TLV320AIC3106](#) data sheet for detailed electrical characteristics of relevant interfaces.

Main supported features are:

- 2 x stereo line in
- Stereo line out
- Stereo headphones driver
- Digital microphone
- Analog microphone

4.7.2 Audio CODEC Signals

Signal	Pin #	Type	Description
DMIC_DATA	175	I/O	Digital microphone data
DMIC_CLK	176	O	Digital microphone clock
LINEIN1_RP	179	A	MIC1 or line1 analog input (right + or multifunction)
LINEIN1_LP	180	A	MIC1 or line1 analog input (left + or multifunction)
LINEIN1_RM	181	A	MIC1 or line1 analog input (right – or multifunction)
LINEIN1_LM	182	A	MIC1 or line1 analog input (left – or multifunction)
LINEIN2_LP	183	A	MIC2 or line2 analog input (left + or multifunction)
LINEIN2_RM	184	A	MIC1 or line1 analog input (right – or multifunction)
LINEIN2_LM	185	A	MIC2 or line2 analog input (left – or multifunction)
LINEIN2_RP	186	A	MIC2 or line2 analog input (right + or multifunction)
LINEOUT_LM	187	A	Left line output (–)
LINEOUT_LP	189	A	Left line output (+)
HPLOUT	190	A	High-power output driver (left +)
LINEOUT_RM	191	A	Right line output (–)
HPROUT	192	A	High-power output driver (right +)
LINEOUT_RP	193	A	Right line output (+)
MICBIAS	196	A	Microphone bias voltage output
MIC_IN_R	197	A	MIC input (right)
MIC_IN_L	198	A	MIC input (left)

Table 4-8 Audio Signals

4.7.3 McASP

Two AM335x McASP interfaces are exposed by the SO-DIM200 connector. The interfaces are muxed with other functionalities. Refer to [PinMux Table 3.2](#) for available PinMux options. Refer to the [Multimedia Audio Serial Port](#) section in Chapter 2 for McASP details.

4.8 UART Interfaces

By default three UART interfaces are supported, refer to [PinMux Table 3.2](#) for further configuration options for the UART interface.

4.8.1 UART Features

The general features of the UART module:

- 16C750 compatibility
- Baud rate from 300 bps up to 3.6864 Mbps

- Auto-baud between 1200 bps and 115.2 Kbps
- Software/hardware flow control
 - Programmable Xon/Xoff characters
 - Programmable Auto-RTS and Auto CTS
- Programmable serial interface characteristics
 - 5, 6, 7, or 8-bit characters
 - Even, odd, mark (always 1), space (always 0), or no parity (non-parity bit frame) bit generation and detection
 - 1, 1.5, or 2 stop bit generation
- False start bit detection
- Line break generation and detection
- Modem control functions (CTS, RTS, DSR, DTR, RI, and DCD)
- Fully prioritized interrupt system controls
- Internal test and loopback capabilities

4.8.2 UART0 Signals

Signal	Pin #	Type	Description
UART0_TX	37	O	UART transmit ^[1]
UART0_RX	35	I	UART receive ^[1]
UART0_RTS		O	UART HW flow control RTS ^[2]
UART0_CTS		I	UART HW flow control CTS ^[2]

Table 4-9 UART0 Signals

4.8.3 UART1 Signals

Signal	Pin #	Type	Description
UART1_TXD	158	O	UART transmit
UART1_RXD	156	I	UART receive
UART1_RTSN	155	O	UART HW flow control RTS
UART1_CTSN	153	I	UART HW flow control CTS

Table 4-10 UART1 Signals

4.8.4 UART3 Signals

Signal	Pin #	Type	Description
UART3_TXD	173	O	UART transmit
UART3_RXD	171	I	UART receive
UART3_RTS		O	UART HW flow control RTS ^[2]
UART3_CTS		I	UART HW flow control CTS ^[2]

Table 4-11 UART3 Signals

Note:

1. UART0 Signals are used by default as a low level debug port
2. Refer to [PinMux Table 3.2](#) for RTS/CTS Options

4.9 SPI

The VAR-SOM-AM33 SPI is based on AM335x McSPIx interfaces. By default one McSPI1 interface is supported. Refer to [PinMux Table 3.2](#) for further McSPI interfaces configuration options.

4.9.1 SPI Features

The general features of the SPI controller are:

- Buffered receive/transmit data register per channel (1 word deep)
- Multiple SPI word access with one channel using a FIFO
- Two DMA requests per channel, one interrupt line
- Single interrupt line, for multiple interrupt source events
- Serial link interface supports:
 - Full duplex / Half duplex
 - Multi-channel master or single channel slave operations
 - Programmable 1-32 bit transmit/receive shift operations.
 - Wide selection of SPI word lengths continuous from 4 to 32 bits
- Up to four SPI channels
- SPI word Transmit / Receive slot assignment based on round robin arbitration
- SPI configuration per channel (clock definition, enable polarity and word width)
- Clock generation supports:
 - Programmable master clock generation (operating from fixed 48-MHz functional clock input)
 - Selectable clock phase and clock polarity per chip select.

4.9.2 McSPI1 Signals

Signal	Pin #	Type	Description
SPI1_SCLK	167	IO	McSPI1 clock
SPI1_D0	163	IO	McSPI1 DO signal
SPI1_D1	165	IO	McSPI1 D1 signal
SPI1_CS0	161	IO	McSPI1 chip select 0 signal

Table 4-12 SPI Signals

4.10 I²C

By default, two I²C interfaces (I2C0, I2C1) are supported, driven by the AM335x controller. Refer to [PinMux Table 3.2](#) for further configuration options for I²C interfaces.

4.10.1 I²C Features

AM335x I²C controller main features are:

The general features of the I2C controller are:

- Compliant with Philips I2C specification version 2.1
- Supports OmniVision Serial Camera Control Bus Protocol (SCCB)
- Supports standard mode (up to 100K bits/s) & fast mode (up to 400K bits/s) .
- Multimaster transmitter/slave receiver mode
- Multimaster receiver/slave transmitter mode
- Combined master transmit/receive and receive/transmit modes
- 7-bit and 10-bit device addressing modes
- Built-in FIFO for buffered read or write
 - I2C0: 32 bytes
 - I2C1: 32 bytes
- Programmable clock generation
- Two DMA channels, one interrupt line

4.10.2 I2C0 Signals

Signal	Pin #	Type	Description
I2C0_SCL	172	IO	I2C0 I ² C clock, open drain ^[1]
I2C0_SDA	174	IO	I2C0 I ² C data, open drain ^[1]

Table 4-13 I2C0 Signals

Note [1]: I2C0 interface is used by some on board devices. Pin configuration for I2C0 signal can't be changed.

4.10.3 I2C0 Address Mapping

The table below summarizes I2C0 address used by on board I²C slave devices:

Device	Address
Audio Codec	0x0011011
PMIC Control	0x0101101
PMIC SmartReflex	0x0010010

Table 4-14 I2C0 Address Mapping

4.10.4 I2C1 Signals

Signal	Pin #	Type	Description
I2C1_SCL	106	IO	I2C1 I ² C clock, open drain
I2C1_SDA	104	IO	I2C1 I ² C data, open drain

Table 4-15 I2C1 Signals

4.11 PWM0

By default, one PWM interface is supported, driven by the AM335 controller, refer to [PinMux Table 3.2](#) for further configuration options for PWM outputs (under “EHRPWM” functions).

4.11.1 PWM0 Signal

Signal	Pin #	Type	Description
EHRPWM0A	159	O	PWM signal

Table 4-16 PWM0 Signal

4.12 Local Bus

The general-purpose memory controller (GPMC) is a unified memory controller dedicated to interfacing external memory devices.

4.12.1 GPMC Features

- Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices
- Asynchronous, synchronous and page mode (only available in non-multiplexed mode) burst NOR flash devices
- NAND Flash
- Pseudo-SRAM devices

Refer to [PinMux Table 3.2](#) for exposed GPMCs

4.13 Touch Screen

VAR-SOM-AM335x touch panel interface can be configured for use in one of the following applications:

- 8 general purpose ADC channels
- 4-wire TSC with 4 general purpose ADC channels
- 5-wire TSC with 3 general purpose ADC channels
- 8-wire TSC

4.13.1 ADC Features

The main features of the TSC_ADC_SS include:

- Support for 4-wire, 5-wire and 8-wire resistive TS panels
- Support for interleaving TS capture and general-purpose ADC modes
- Programmable FSM sequencer that supports 16 steps:
 - Software register bit for start of conversion
 - Optional start of conversion HW synchronized to Pen touch or external HW event (but not both)
 - Single conversion (one-shot)
 - Continuous conversions
 - Sequence through all input channels based on a mask
 - Programmable OpenDelay before sampling each channel
 - Programmable sampling delay for each channel
 - Programmable averaging of input samples - 16/8/4/2/1
 - Differential or singled ended mode setting for each channel
 - Store data in either of two FIFO groups
 - Option to encode channel number with data
 - Support for servicing FIFOs via DMA or CPU
 - Programmable DMA Request event (for each FIFO)
 - Dynamically enable or disable channel inputs during operation
 - Stop bit to end conversion
- Support for the following interrupts and status, with masking:
 - Interrupt for HW pen (touch) event
 - Interrupt for HW Pen Up event
 - Interrupt after a sequence of conversions (all non-masked channels)
 - Interrupt for FIFO threshold levels
 - Interrupt if sampled data is out of a programmable range
 - Interrupt for FIFO overflow and underflow conditions
 - Status bit to indicate if ADC is busy converting

4.13.2 Touch-screen Controller Signals

Signal	Pin #	Type	Description
AIN0 (TSPX)	28	A	Touch screen X plus
AIN1 (TSPY)	30	A	Touch screen Y plus
AIN2 (TSMX)	27	A	Touch screen X minus
AIN3 (TSMY)	25	A	Touch screen Y minus

AIN4	32	A	Analog input
AIN5	34	A	Analog input
AIN6	29	A	Analog input
AIN7	31	A	Analog input

Table 4-17 Touch Panel Signals

4.14 General Purpose I/O

Most of the SoM's IO pins can be used as GPIOs.

See Chapter 3, [PinMux Table 3.2](#) for a complete SoM connectors signal list and GPIO multiplexing.

4.14.1 Default GPIO Signals

Signal	Pin #	Type	Description
GPIO_0_3	157	I/O	General purpose IO
GPIO_3_7	111	I/O	General purpose IO
GPIO_3_8	160	I/O	General purpose IO
GPIO2_18	66	I/O	General purpose IO
GPIO3_10	70	I/O	General purpose IO
GPIO3_9	72	I/O	General purpose IO

4.15 General System Control

4.15.1 Boot Options

The boot option signal configures the boot sequence of the VAR-SOM-AM33:

Not Connected: First boot device is an on board NAND flash interface, if failed, MMC0 followed by UART0 are used as a boot device.

Logic '1': boot device is an off board SD Card (using MMC/SD/SDIO2 interface), if failed, UART0 is used as a boot device.

Boot selection signal is shared with LCD_DATA2. A 2.2K pull up should be used if Logic'1' is required

4.15.2 SYS_RESETh

Logic '0' will force device reset.

4.15.3 VCC3V3

A VIO signal (3.3V), indicating that boot sequence has started and device input can be driven by external component

4.15.4 General System Control Signals

Signal	Pin #	Type	Description
SYS_BOOT(LCD_D ATA2)	17	I/O	System boot option select
SYS_RESETh	129	I	System hardware reset

VAR-SOM-AM33 SYSTEM ON MODULE

VCC_3V3	170	O	VIO signal, indicating that voltage can be applied for VAR-SOM-AM33 pins
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Table 4-18 General System Signals

4.16 Power

4.16.1 Power Supply

Signal	Pin #	Type	Description
Vin	132, 134, 136, 138, 140, 142, 144,	Power In	VAR-SOM-AM33 Single DC-IN Supply voltage Voltage range: 3.3 +/- 5%
VIO	170	Power Out	
VBCKUPBAT	169	Power In	RTC power supply

Table 4-19 Power Supply Pins

4.16.2 Ground

Signal	Pin #	Type	Description
GND	7,8,18 ,23,26 ,33,36 ,42,45 ,52,57 ,69,75 ,89,90 ,95,96 ,102,1 05,12 2,123, 125,1 30,13 1,133, 143,1 45,		Digital ground
AGND	177,1 78,18 8,194, 195,1 99,20 0	Power	Analog GND

Table 4-20 Ground Pins

5 Absolute Maximum Characteristics

Power Supply	Min	Max	Unit
Main Power Supply, DC-IN	-0.3	3.5	V

Table 5-1 Absolute Maximum Characteristics

6 Operational Characteristics

6.1 Power supplies

	Min	Typical	Max	Unit
Main Power Supply, DC-IN	-5%	3.3	+5%	V

Table 6-1 Power Supplies Operational Characteristics

6.2 Power Consumption

TBD

7 DC Electrical Characteristics

Parameter	Min	Typical	Max	Unit
V_{IH}	2			V
V_{IL}			0.8	V
V_{OH}	$V_{IN}-0.2$			V
V_{OL}			0.2	V

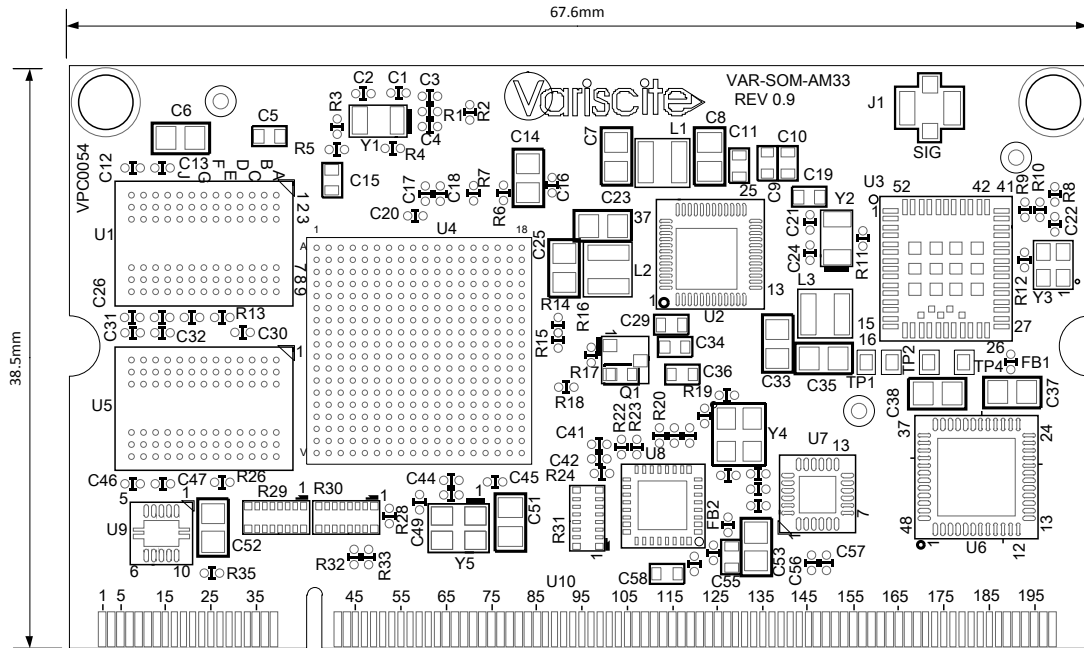
Table 7-1 DC Electrical Characteristics

8 Environmental Specifications

	Min	Max
Commercial Operating Temperature Range	0 °C	+70 °C
Extended Operating Temperature Range	-20 °C	+70 °C
Industrial Operating Temperature Range	-40 °C	+80 °C
Referring MIL-HDBK-217F-2 Parts Count Reliability Prediction Method Model: 50Deg Celsius, Class B-1, GM 50Deg Celsius, Class B-1, GB	121 Khrs > 1400 Khrs >	
Shock Resistance	50G/20 ms	
Vibration	20G/0 - 600 Hz	

9 Mechanical Drawings

Top View



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